

WEST**End of Result Set** **Generate Collection**

L1: Entry 3 of 3

File: USPT

Apr 24, 2001

US-PAT-NO: 6222113DOCUMENT-IDENTIFIER: US 6222113 B1

TITLE: Electrically-isolated ultra-thin substrates for thermoelectric coolers

DATE-ISSUED: April 24, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ghoshal; Uttam Shyamalindu	Austin	TX		

US-CL-CURRENT: 136/201; 136/203, 62/3.3, 62/3.61, 62/3.7

CLAIMS:

What is claimed is:

1. A thermoelectric cooling apparatus comprising:

at least one thermal sink;

at least one thermoelectric cooling element situated to be coupled to said thermal sink; and wherein said thermal sink comprises a semiconductor material having a plurality of doped regions.

2. The thermoelectric cooling apparatus, as claimed in claim 1, wherein said doped regions form at least one diode.

3. The thermoelectric cooling apparatus, as claimed in claim 2, wherein said at least one diode is reverse biased.

4. The thermoelectric cooling apparatus, as claimed in claim 1, wherein said doped regions form one or more discrete electrical devices.

5. The thermoelectric cooling apparatus, as claimed in claim 1, wherein said doped regions form one or more integrated circuits.

6. The thermoelectric cooling apparatus, as claimed in claim 5, wherein said integrated circuits are capable of controlling the operation of said thermoelectric cooling apparatus.

7. The thermoelectric cooling apparatus, as claimed in claim 1, wherein the thickness of said thermal sink is less than 10 microns.

8. The thermoelectric cooling apparatus, as claimed in claim 1, wherein the thickness of said thermal sink is less than 1 millimeter.

9. The thermoelectric cooling apparatus, as claimed in claim 1, further comprising:

a second thermoelectric element; and

a junction positioned between and coupled to said thermoelectric element and said second thermoelectric element.

10. The thermoelectric cooling apparatus, as claimed in claim 9, wherein said junction is said thermal sink.

11. The thermoelectric cooling apparatus, as claimed in claim 1, wherein said thermoelectric element is a peltier device.

12. The thermoelectric cooling apparatus, as claimed in claim 1, wherein said thermoelectric cooling apparatus is associated with at least one vehicle integrated circuit device.

13. The thermoelectric cooling apparatus, as claimed in claim 1, wherein said thermoelectric cooling apparatus is associated with at least one vehicle occupant cooling system.

14. The thermoelectric cooling apparatus, as claimed in claim 1, wherein said thermoelectric cooling apparatus is associated with at least one food refrigeration system.

15. The thermoelectric cooling apparatus, as claimed in claim 1, wherein said thermoelectric cooling apparatus is associated with at least one microelectromechanical system (MEMS).

16. The thermoelectric cooling apparatus, as claimed in claim 1, further comprising:

a first thermal sink of a first nominal temperature;

a second thermal sink of a second nominal temperature being relatively greater than the first temperature; and wherein said thermoelectric element is situated to be coupled to said first and second thermal sinks;

and wherein at least one of said first and second thermal sinks comprises a semiconductor material having a plurality of doped regions.

17. A method of fabricating a thermoelectric cooling apparatus comprising:

forming at least one thermal sink of a semiconductor material having a plurality of doped regions; and

coupling a thermoelectric element to the thermal sink.

18. The method, as claimed in claim 17, further comprising:

forming a diode in the semiconductor material of the thermal sink.

19. The method, as claimed in claim 18, further comprising:

enabling the diode in a reverse biased state.

20. The method, as claimed in claim 17, further comprising:

forming one or more discrete electrical devices in the semiconductor material of the thermal sink.

21. The method, as claimed in claim 17, further comprising:

forming one or more integrated circuits in the semiconductor material of the thermal sink.

22. The method, as claimed in claim 21, further comprising:

enabling the integrated circuits to control the operation of said thermoelectric cooling apparatus.

23. The method, as claimed in claim 17, further comprising:

forming a junction positioned between and coupled to the thermoelectric element and a second thermoelectric element.

24. The method, as claimed in claim 23, wherein the junction is the thermal sink.

25. The method, as claimed in claim 17, wherein the thermoelectric element is a peltier device.

26. The method, as claimed in claim 17, wherein the step of forming the thermal sink includes the step of forming the thermal sink having a thickness less than 10 microns.

27. The method, as claimed in claim 17, wherein the step of forming the thermal sink includes the step of forming the thermal sink having a thickness less than 1 millimeter.

28. A thermal sink situated to be coupled to a thermoelectric element comprising a semiconductor material having a plurality of doped regions.

29. The thermal sink, as claimed in claim 28, wherein said doped regions form at least one diode.

30. The thermal sink, as claimed in claim 29, wherein said at least one diode is reverse biased.

31. The thermal sink, as claimed in claim 28, wherein said doped regions form one or more discrete electrical devices.

32. The thermal sink, as claimed in claim 28, wherein said doped regions form one or more integrated circuits.

33. The thermal sink, as claimed in claim 32, wherein said integrated circuits are capable of controlling the operation of said thermoelectric element.

34. The thermal sink, as claimed in claim 28, wherein the thickness of said thermal sink is less than 10 microns.

35. A method of fabricating a thermal sink adapted to be coupled to a thermoelectric element of a thermoelectric cooling apparatus comprising:

providing a semiconductor material; and

forming a plurality of doped regions in the semiconductor material.

36. The method, as claimed in claim 35, further comprising:

forming a diode in the semiconductor material.

37. The method, as claimed in claim 35, further comprising:

forming one or more discrete electrical devices in the semiconductor material.

38. The method, as claimed in claim 35, further comprising:

forming one or more integrated circuits in the semiconductor material.

39. The method, as claimed in claim 35, further comprising:

forming a contact on the semiconductor material for coupling the thermal sink to the thermoelectric element.

40. The method, as claimed in claim 35, further comprising:

forming a conductive layer on the semiconductor material for coupling the thermal sink to an object.

41. The method, as claimed in claim 35, wherein the thickness of the thermal sink is less than 10 microns.

42. The method, as claimed in claim 35, wherein the thickness of the thermal sink is less than 1 millimeter.